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Title: Future computer Architectures: Computing in Memory

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Abstract:
Emerging applications, such as data-intensive/bigdata applications and internet-of-things (IoT), are extremely demanding in terms of storage and computing power. These applications require computing power which was typical of supercomputers a few years ago, but with constraints on size, power consumption and guaranteed response time which are typical of the embedded applications. Today's computing systems, based on von Neumann (VN) architectures, are mainly rely on many parallel (mini-)cores with a shared SRAM cache (parallel CPUs, GPUs, SIMD-VLIWs, and vector processors). It is well recognised that such solutions suffer from major limitations such as a decreased performance acceleration per core, increased power consumption, and limited system scalability. These makes them uncappable to deliver the required services for emerging applications.

This talk will first address the CMOS scaling and its impact on different aspects of IC and electronics; the major limitations and challenges the scaling is facing will be shown and the need of a new technology will be motivated. Thereafter, an overview of computing systems, developed since the introduction of Stored program computers by John von Neumann in the forties, will be given. Shortcomings of today's architectures including their limitations will be highlighted, and the need for a new architecture will be discussed. Possible future architectures will be highlighted and a new architecture paradigm, referred to as "Computation-In-Memory (CIM)" will be introduced; it is based on the integration of the storage and computation in the same physical location (using a crossbar topology) and the use of non-volatile resistive-switching technology, based on memristors, instead of CMOS technology. Some aspects of CM architecture and its huge potential of in realizing order of magnitude improvement will be illustrated by comparing it with the state-of-the art architectures for different data-intensive applications.

Bio: Said Hamdioui (http://www.ce.ewi.tudelft.nl/hamdioui/) is a chair professor on dependable and emerging computing technologies at Delft University of Technology (TUDelft), Delft, The Netherlands. Prior to joining TUDelft, Hamdioui worked for intel (CA), Philips Semiconductors R&D (France) and Philips/ NXP Semiconductors (the Netherlands). His research focuses on two domains: Dependable CMOS nano-computing (including Reliability, Testability, Hardware Security) and emerging technologies and computing paradigms (including 3D stacked ICs, memristors for logic and storage, in-memory-computing for big-data applications).

Hamdioui owns one patent and has published one book and co-authored over 170 conference and journal papers. He has consulted for many companies (such as Intel, ST, Altera, Atmel, Renesas, …) in the area of memory testing and has collaborated with many industry/research partners (examples are Intel, IMEC, NXP, Intrinsic ID, DS2, ST Microelectronics, Cadence, Politic di Torino, etc) in the field of dependable nano-computimng and emerging technologies. He is strongly involved in the international community as a member of organizing committees (e.g., general chair, program chair, etc) or a member of the technical program committees of the

leading conferences. He delivered dozens of keynote speeches, distinguished lectures, and invited presentations and tutorial at major international forums/conferences/schools and at leading semiconductor companies. Hamdioui is a Senior member of the IEEE, Associate Editor of IEEE Transactions on VLSI Systems (TVLSI), and he serves on the editorial board of IEEE Design & Test, and of the Journal of Electronic Testing: Theory and Applications (JETTA). He is also member of AENEAS/ENIAC Scientific Committee Council (AENEAS =Association for European NanoElectronics Activities).