Biography Dr. **Carmen G. Almudever**

Dr. **Carmen G. Almudever** is an Assistant Professor at the Computer Engineering Lab of TU Delft. She holds a PhD in Electronic Engineering from Polytechnic University of Catalonia, Spain. During her PhD she was working on "beyond-CMOS" technologies such as carbon nanotubes and memristive devices as well as on novel reconfigurable architectures and dynamic computing systems. In 2102 she received a fellowship from Intel (Doctoral Student Honor Programme). She is currently responsible for the quantum plane architectures, which involves the definition of the infrastructure needed for the efficient mapping of quantum circuits and routing of quantum states. Her main research interests include quantum computer architecture, fault-tolerant quantum operations, mapping of large-scale quantum circuits and quantum plane architectures.

WHAT IS QUANTUM COMPUTNG ALL ABOUT?

A quantum computer holds the promise to solve efficiently some classes of computational problems that are intractable for a classical computer by exploiting fundamental quantum phenomena such are superposition and entanglement. Some examples of those problems are big data and optimization problems, chemical simulation and cryptography. The most popular example is the use of Shor's algorithm for factorizing large numbers and its possible application for breaking public-key cryptography schemes such as RSA. Using such an algorithm a quantum computer could factorize a 2000-bit number in a bit more than one day, whereas a data center of approx. 400.000 Km^2 built with the fastest today's supercomputer would required around 100 years.

In this talk, we will provide an overview of quantum computing as compared to classical computing and introduce the basic concepts of quantum error correction. We will also address the main challenges when building a large-scale quantum computer that includes: i) to improve quantum technologies, ii) to implement scalable quantum processors and control electronics, and iii) to develop an overall system architecture.
