Approximate Computing for low-power: surveys and challenges

Approximate computing is an (re-)emerging paradigm for building highly power-/energy-efficient on-chip systems. In the past, well studied techniques like Digital Voltage and Frequency Scaling (DVFS) and power-gating have been the primary research focus for reducing power consumption of on-chip systems. These techniques essentially assume that the requirement of perfect or precise computing results at all stages. However, as the process technology shrinks and the per-transistor performance/power efficiency is not keeping pace with known power-reduction techniques at various abstraction levels, continuing to support precise computing is most likely not a way to solve upcoming energy-efficiency challenges. This stimulates the exploration of new directions that provide a path forward for the electronics / computing industry.

Relaxing the bounds of precise computing provides new opportunities that may bear orders of magnitude in performance/power benefits. Recently, the investigations by Microsoft, Intel, and other research groups have shown that there is a large body of resource-hungry applications from prevalent and emerging application domains (like: data analytics and data mining, recognition and machine learning, web searches, image and video processing, computer vision, mobile computing, artificial intelligence, etc.) that is amenable to approximate computing due to applications' inherent resilience to approximation errors.

In this presentation, we will go through the motivation of employing approximate computing through various stages of the design flow. We will understand what techniques have been proposed in literature and their potential in tackling the power challenges. The talk will also present some challenges in this field.

Bio:

Akash Kumar received the B.Eng. degree in computer engineering from the National University of Singapore (NUS), Singapore, in 2002, the Master's degree in technological design with a minor in embedded systems jointly from NUS and the Eindhoven University of Technology (TUe), Eindhoven, The Netherlands, in 2004, and the Ph.D. degree in electrical engineering with a minor in embedded systems jointly from TUe and NUS, in 2009. He was with the Department of Electrical and Computer Engineering, NUS, from 2009 to 2015. He is currently with the Technische Universität Dresden (TUD), Germany, where he directs the Chair for Processor Design. He has authored over 120 papers in leading international electronic design automation journals and conferences in his research areas. His current research interests include design, analysis, and resource management of low-power and fault-tolerant embedded multiprocessor systems, with special focus on approximate computing. Dr. Kumar was a recipient of the best paper award nominations, including the Conference on Field Programmable Logic and Applications (FPL) in 2014, GLSVLSI in 2014, SC in 2015, and the Design, Automation & Test in Europe Conference (DATE) in 2015 and 2017. He is or has been a Technical Program Committee Member of major conferences in the design automation and field-programmable gate array design area, such as the DAC, DATE, ASPDAC, FPL, FPT, CASES.